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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/668,211

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Hiroyuki Ohta

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EXAMINER

LINDSAY JR, WALTER LEE

ART UNIT

PAPER NUMBER

2812

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

AD

Office Action Summary	Application No. 10/668,211	Applicant(s) OHTA, HIROYUKI	
	Examiner Walter L. Lindsay, Jr.	Art Unit 2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
 4a) Of the above claim(s) 16-19 is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-4 and 9 is/are rejected.
- 7) ☒ Claim(s) 5-8 and 10-15 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☒ All b) ☐ Some c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

This Office Action is in response to an Election filed on 10/07/2004.

Currently, claims 1-19 are pending. Claims 16-19 have been withdrawn from consideration.

Election/Restrictions

1. Applicant's election without traverse of claims 1-15 in the reply filed on 10/07/2004 is acknowledged.
2. Claims 16-19 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected device, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 10/07/2004.

Specification

3. The disclosure is objected to because of the following informalities: on page 2 line 19, "leak" should be "leakage", and on page 16, "1.011 k Ω " needs to be stated clearly.

Appropriate correction is required.

4. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 1-3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deshpande et al. (U.S. Patent No. 6,512,266 filed 7/11/2001) in view of Chen (U.S. Patent No. 6,093,629 dated 7/25/2000).

Deshpande shows the method as substantially claimed in Figs. 2A-2G and corresponding text as: a gate electrode (14) traversing a corresponding one of the active regions (10), and forming extension regions of source/drain (20) in the active region on both sides of said gate electrode (Fig. 2A)(col. 7, lines 50-59); depositing first (22) and second insulating films (24) having different etching characteristics ((22) is an oxide layer and (24) is a nitride or oxynitride layer) on the silicon substrate, said first and second insulating films covering sidewalls of said gate electrode, and anisotropically

etching (reactive ion etching) said first and second insulating films to form a side wall spacer (25, 24) on the side walls of each gate electrode (fig. 2C)(col. 8, lines 11-39); selectively etching said first insulating film of the side wall spacer to form a retraction portion (26) retracted from a surface of said second insulating film on a gate electrode side and on a silicon substrate side (Fig. 2E)(col. 8, lines 45-53); implanting ions into the silicon substrate by using the side wall spacer as a mask to form source/drain regions (16) in the silicon substrate (Fig. 2D)(col. 8, lines 40-44); and depositing metal capable of silicidation over the silicon substrate and performing a silicidation reaction and form silicide regions (col. 9, lines 5-12) (claim 1). Deshpande teaches that the selective etching at said step (c) is isotropical etching (col. 8, lines 45-53) (claim 2). Deshpande teaches that the first insulating film is made of silicon oxide (col. 7, line 66-col. 8, line 2), said second insulating film is made of silicon nitride (col. 8, lines 28-39), and said step (c) selectively wet-etches silicon oxide with dilute hydrofluoric acid aqueous solution (col. 8, lines 45-53) (claim 3). Deshpande shows the method as substantially claimed in Figs. 2A-2G and corresponding text as: a gate electrode (14) traversing a corresponding one of the active regions (10), and forming extension regions of source/drain (20) in the active region on both sides of said gate electrode (Fig. 2A)(col. 7, lines 50-59); depositing first (22) and second insulating films (24) having different etching characteristics ((22) is an oxide layer and (24) is a nitride or oxynitride layer) on the silicon substrate, said first and second insulating films covering sidewalls of said gate electrode, and anisotropically etching (reactive ion etching) said first and second insulating films to form a side wall spacer (25, 24) on the side walls of each gate

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electrode (fig. 2C)(col. 8, lines 11-39); selectively etching said first insulating film of the side wall spacer to form a retraction portion (26) retracted from a surface of said second insulating film on a gate electrode side and on a silicon substrate side (Fig. 2E)(col. 8, lines 45-53); implanting ions into the silicon substrate by using the side wall spacer as a mask to form source/drain regions (16) in the silicon substrate (Fig. 2D)(col. 8, lines 40-44); and depositing a third insulating film (28) on the silicon substrate, the third insulating film entering the retraction portion and burying the retraction portion (Fig. 2F) (col. 8, lines 58-63) (claim 9).

Deshpande lacks anticipation only in not explicitly teaching that: 1) a gate electrode is formed over each of a plurality of active regions defined in a silicon substrate, said gate electrode traversing a corresponding one of the active regions, and forming extension regions of source/drain in the active region on both sides of said gate electrode (claims 1 and 9).

Chen teaches a CMOS integrated circuit with both PMOS and NMOS devices. The PMOS device (6) of Chen is formed in the n-well (12) while the NMOS device (8) is formed in the p-well (14) (col. 3, lines 25-39). Field oxide (16) separates these two regions (col. 3, lines 7-15). The devices are formed in such a way as to increase device density, which leads to improved circuit performance and reliability as well as reduced cost.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify the method and structure shown in Deshpande by forming a gate electrode over each of a plurality of active regions defined in a silicon

substrate, as taught by Chen, with the motivation that Chen forms the device in such a way that it increases device density, which leads to improved circuit performance and reliability as well as reduce cost.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Deshpande et al. (U.S. Patent No. 6,512,266 filed 7/11/2001) in view of Chen (U.S. Patent No. 6,093,629 dated 7/25/2000) as applied to claim 1 above, and further in view of Deshpande et al. (U.S. Patent No. 6,512,266 filed 7/11/2001) (first embodiment).

Deshpande as modified by Chen shows the method substantially as claimed and as described in the preceding paragraphs

Deshpande as modified by Chen lacks anticipation only in not explicitly teaching that: 1) the step (c) side-etches said first insulating film at least by 10 nm and at most 0.6 times a width of the side wall spacer (claim 4).

Deshpande teaches a CMOS device in a first embodiment that is forms an L-shaped spacer (Figs. 1A-1F). The L-shaped structures (23) are recessed below the level of the second spacer and the gate electrode (col. 6, lines 38-48). The L-shaped structure is recessed from the edge of the second spacer in the lateral direction also (col. 6, lines 38-48). The thickness of the divot is from 4 to about 80 nm in depth (col. 7, lines 4-7). The use of the L-shaped spacer is used to help in the reduction of parasitic capacitance and to improve the ring oscillation delay.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made to modify the method shown in the second embodiment of Deshpande by side etching the first insulating film by at least 10 nm and at most 0.6

times a width of the side wall spacer as taught in the first embodiment of Deshpande, with the motivation that Deshpande teaches the reduction of parasitic capacitance and improvement shown in the ring oscillation delay.

Allowable Subject Matter

9. Claims 5-8 and 10-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...wherein the plurality of active regions include n- and p-channel regions, said step (d) includes a step of obliquely implanting n-type impurity ions into the n-channel region, while p-type impurity ions are implanted into the p-channel region only at an angle nearer to a substrate normal than the oblique ion implantation, as required by claims 5 and 10;

...wherein said step (d) includes a step of obliquely implanting n-type impurity ions into the n-channel region and a step of vertically implanting n-type impurity ions into the n-channel region, as required by claims 6 and 11 ;

...wherein said step (e) sputters Co or Ni on the silicon substrate and also in the retraction portion on the silicon substrate and also in the retraction portion on the silicon substrate side, and forms the silicide region also on the silicon substrate under the

retraction portion and a thicker silicide region on the silicon substrate outside of the side wall spacer, as required by claim 7;

(f) after said step (e), depositing a third insulating film on the silicon substrate, the third insulating film entering the retraction portion and burying the retraction portion, as required by claims 8, 12 and 14; and

...wherein the metal capable of silicidation is cobalt or nickel, as required by claims 13 and 15.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John F Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL


November 18, 2004